AW-XH325

IEEE 802.11 a/b/g/n/ac/ax Wi-Fi

+ Bluetooth 5.2 Combo SIP Module

Layout Guide

Rev. 01

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
01	2023/05/11	● Initial Version	Barry Tsai	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-XH325 layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

1. GENERAL RF GUIDELINES
2. Ground Layout
3. Power Layout
4. Digital Interface
5. RF Trace
6. Antenna
7. Antenna Matching
8. GENERAL LAYOUT GUIDELINES
9. LGA Module stencil and Pad opening Suggestion
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11. Mechanical Characteristics
12. SMT Process Suggestion
13. Module IC SMT preparation
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15. THE OTHER LAYOUT GUIDE INFORMATION
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1. GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:

- Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
- Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
- Keep all trace routing inside the ground plane area by at least the width of a trace.
- Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:

- Do not route any digital or analog signal traces between the RF traces and the reference ground.
- Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
- Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:

- Confirm antenna ground keep-outs.
- Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
- Do not use thermals on RF traces because of their high loss.
- The RF traces between AW-XH325 C0_ANT pin and C1_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

2. Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

5. RF Trace

The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.

- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

If the customers have any problem in calculation of trace impedance, please contact AzureWave.

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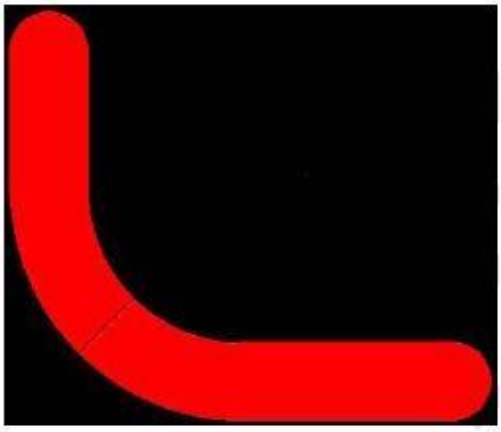
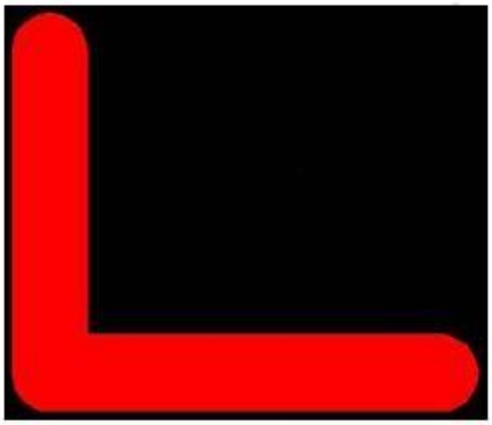
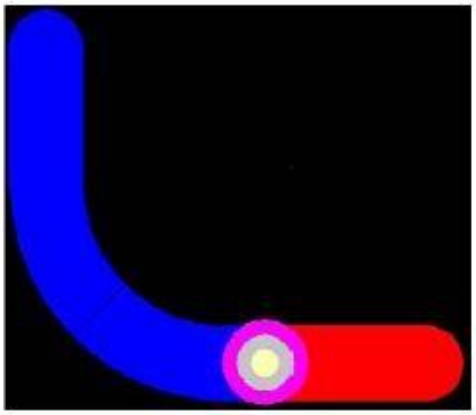


Correct RF trace



Right-angled corner



Via on RF trace

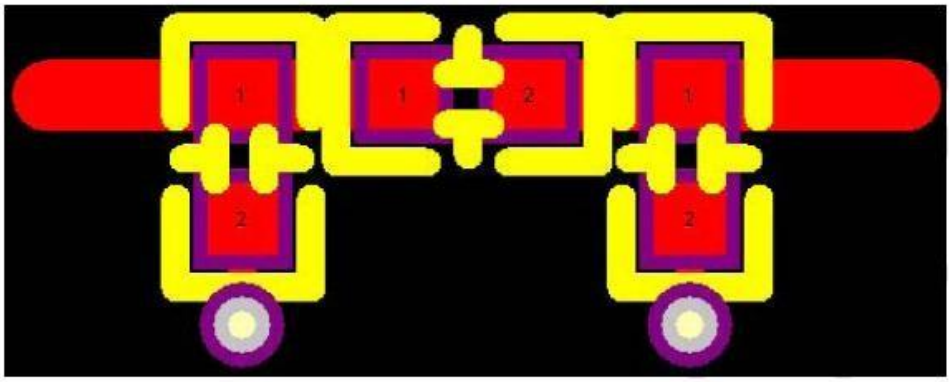
Incorrect RF trace

6. Antenna

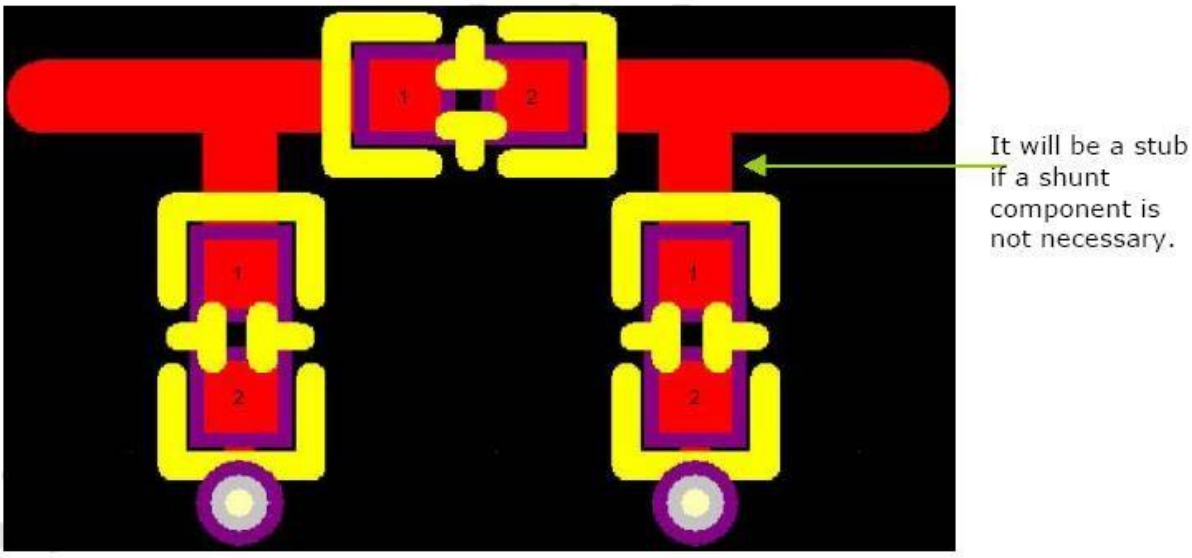
- All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

7. Antenna Matching

- PCB designer should reserve an antenna matching network for post tuning to ensure the antenna



Correct layout for antenna matching



Incorrent layut for antenna matching

8. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:

- Keep analog and digital circuits in separate areas.
- Identify all high-bandwidth signals and their return paths. Treat all critical signals as current performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.
- Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
- Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.
- However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
- Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.

2. Consider the following with respect to ground and power supply planes:

- Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
- Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
- Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

3. Consider these power supply decoupling practices:

- Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a

copper trace. Instead, make the connection directly to the associated planes using vias.

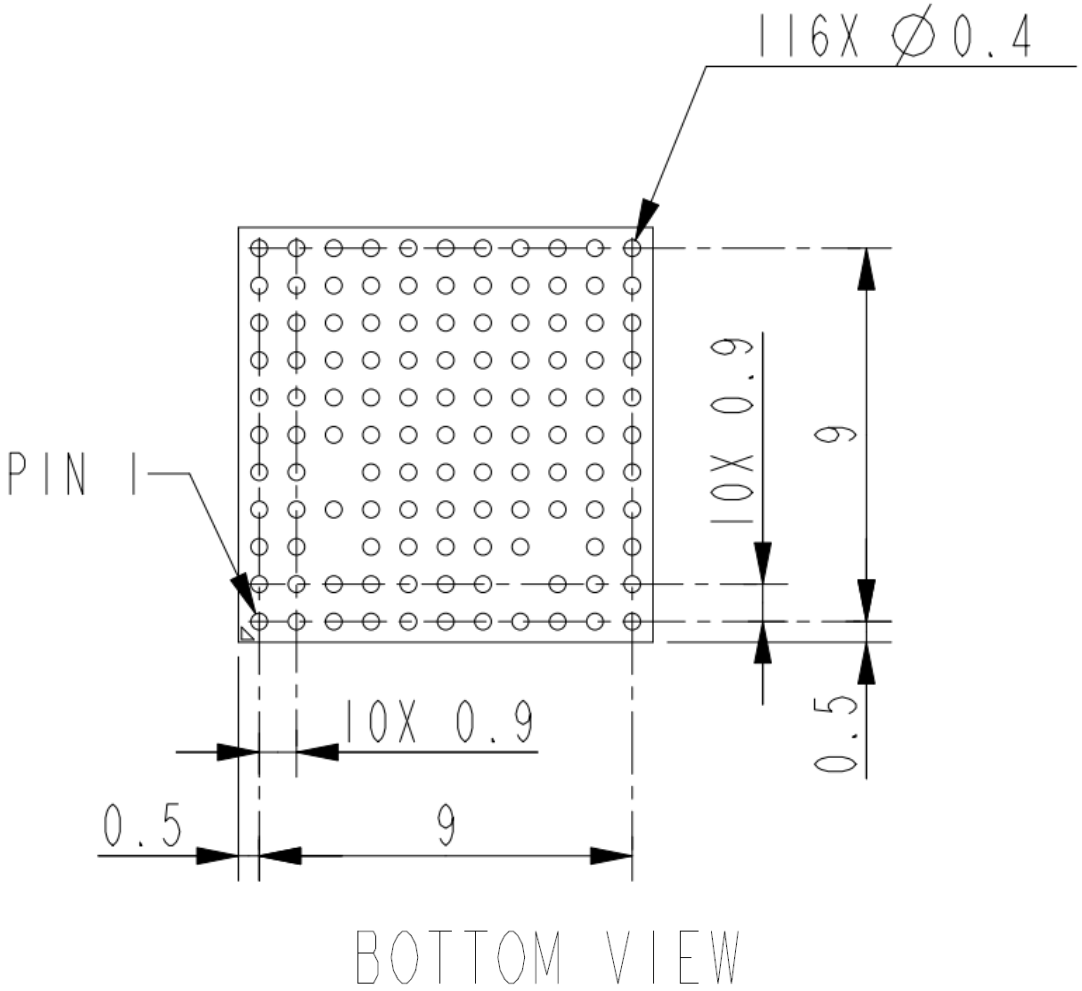
- Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

9. LGA Module stencil and Pad opening Suggestion

- Stencil thickness：0.08~0.10mm
- Function Pad opening size suggestion: Max. 1:1

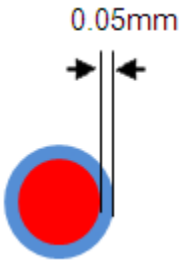
PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- 10x10mm Solder Printer Opening Reference:
- Solder Paste: Need to use type 5 paste (powder 5).



10. LGA Pad Opening Suggestion

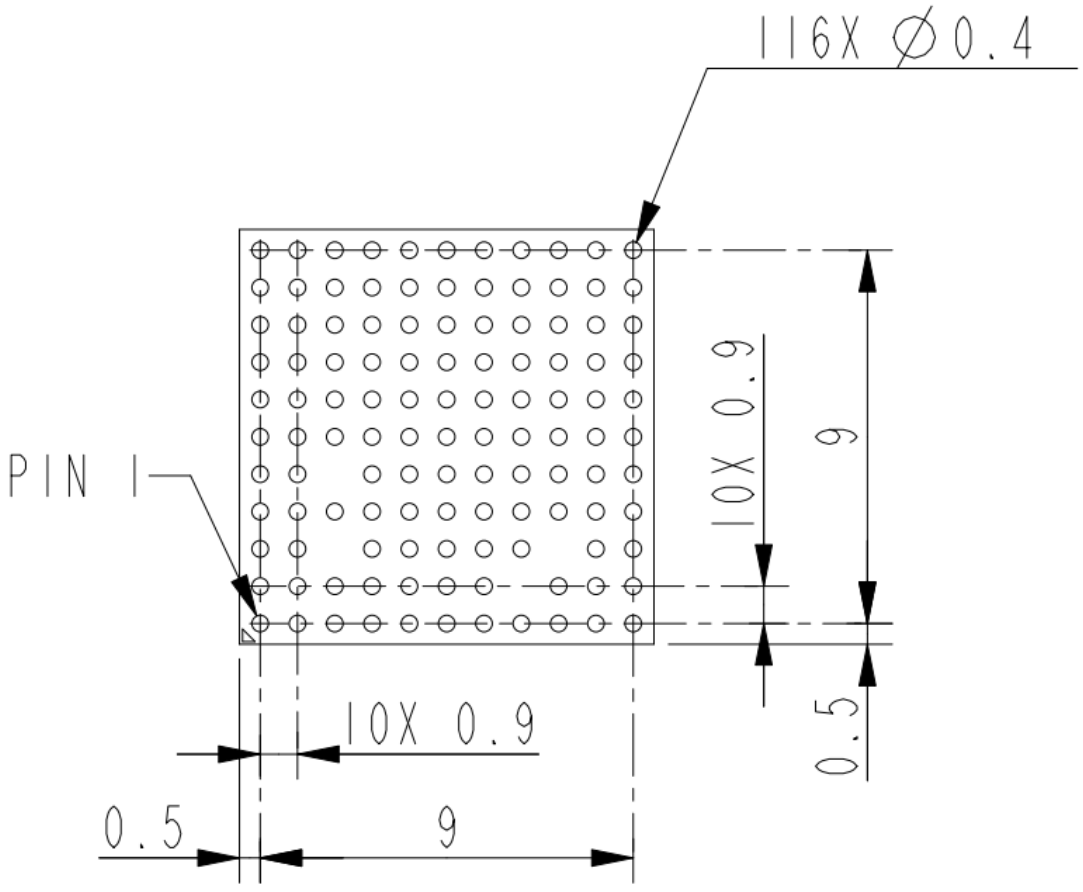
- IF Cu Pad size : 0.85mm
- Pad opening suggestion: 0.75mm



11. Mechanical Characteristics

- The size of the 4x4mm LGA package module is listed below:

PCB Layout Footprint



Bottom VIEW

12. SMT Process Suggestion

- Reflow soldering profile

Table 4-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 4-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

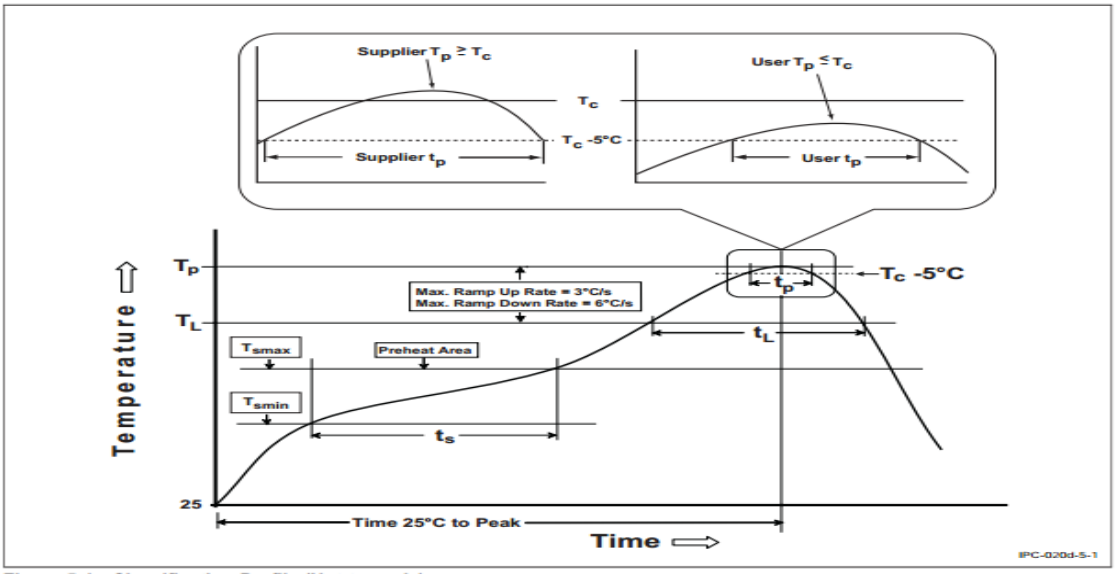


Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note: 1. Recommend to supply N_2 for reflow oven

2. N_2 atmosphere during reflow (O_2<300ppm)

13. Module IC SMT preparation

- Shelf life in sealed bag: 12 months, at <30℃ and <60% relative humidity (RH)
- After bag is opened, devices that will be

13.1 Baked for 24 hours at 125+-5℃ with tray

13.2 Re-baked required after last baked with window time 168 hours

- Baking Condition:

13.3 High Temperature Carriers

13.3.1 Exceeding Floor Life > 72 hours: bake @125℃ 8 hours

13.3.2 Exceeding Floor Life ≦ 72 hours: bake @125℃ 6 hours

13.4 Low Temperature Carriers

13.4.1 Exceeding Floor Life > 72 hours: bake @60℃ ≦5% RH 6 days

13.4.2 Exceeding Floor Life ≦ 72 hours: bake @60℃ ≦5% RH 3 days

- Recommend to oven bake with N2 supplied
- Recommend end to reflow oven with N2 supplied
- Recommend to store at ≦10% RH with vacuum packing
- If SMT process needs twice reflow:

13.5 Process flow: (1) Bottom side SMT and reflow → (2) Top side SMT and reflow

13.5.1 Case 1: Module IC mounted on Top side. Need to bake when bottom side process over 168 hours window time

13.5.2 Case 2: Module IC mounted on bottom side, follow normal bake rule before process

Note: Window time means from last bake end to next reflow start that has 168 hours space.

14. Repair:

14.1 Tool and Material:

14.1.1 Soldering Station

14.1.2 Soldering braid

14.1.3 Iron

14.1.4 Stencil fixture for Module

14.1.5 Soldering Pasts

14.2 Stencil Opening size:

14.2.1 Stencil thickness: 0.1mm(100um)

14.2.2 Stencil pad size opening: Footprint 100%

14.3 Repair Steps:

14.3.1 Before repair, the product need to baking 2 hrs(125℃).

14.3.2 Using soldering station to de-mount the module.

14.3.3 Using soldering braid and Iron to clean solder of pads.

14.3.4 Using stencil fixture and Soldering pasts to pasts on the pads.

14.3.5 Take the module to put it on the main board.

14.3.6 Using soldering station to mount the module.

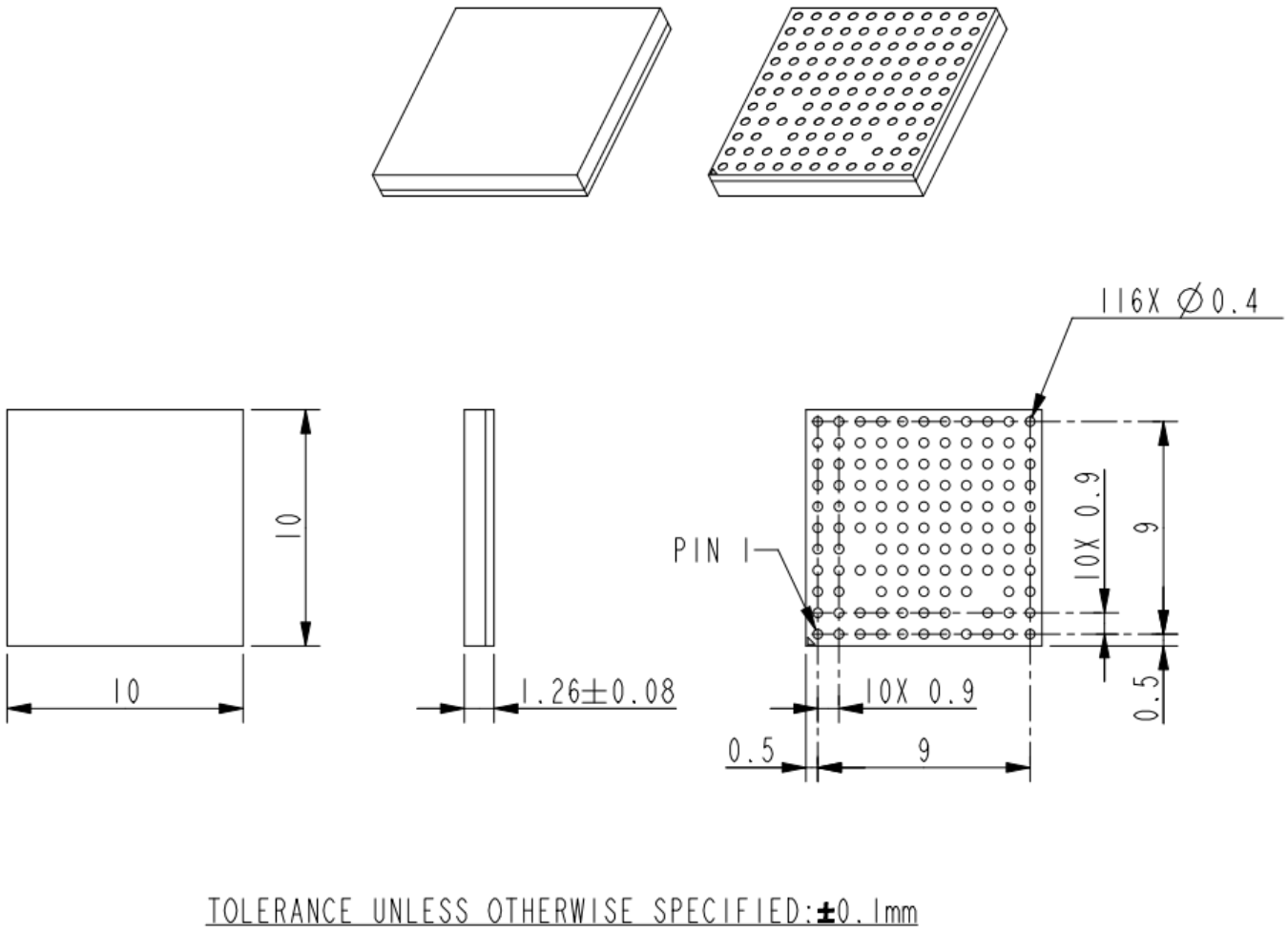
14.3.7 Retest the product.

15. The other layout guide Information

- Make sure every power traces have good return path (ground path).
- Connect the input pins of unused internal regulators to ground.
- Leave the output pins of unused internal regulators floating.
- High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.
- Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
- Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).
- Discuss with AzureWave Engineer after you finish schematic and layout job.

16. Mechanical Drawing

•Package Outline Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

·Bottom View of PCB Layout Foot Print